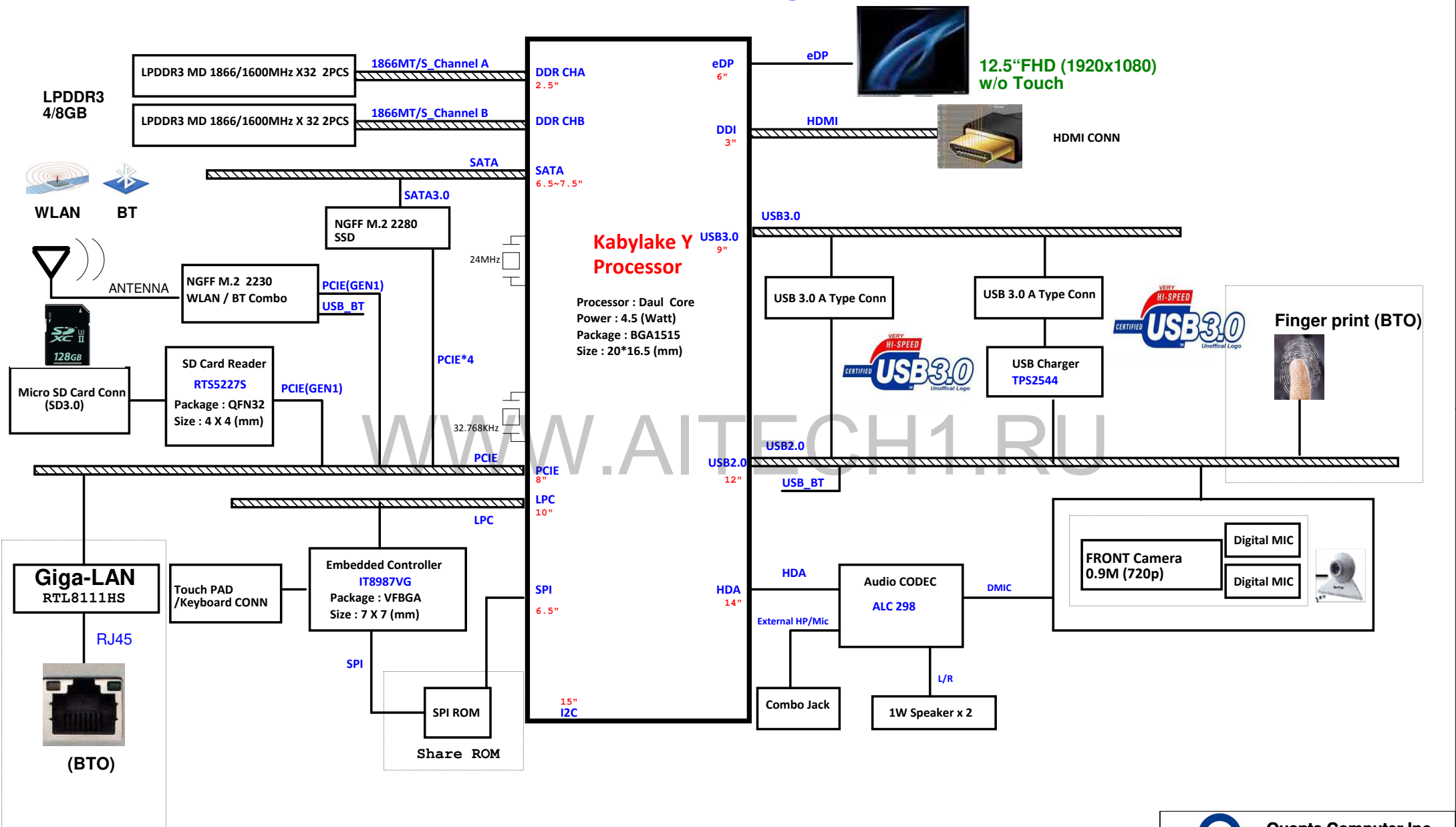
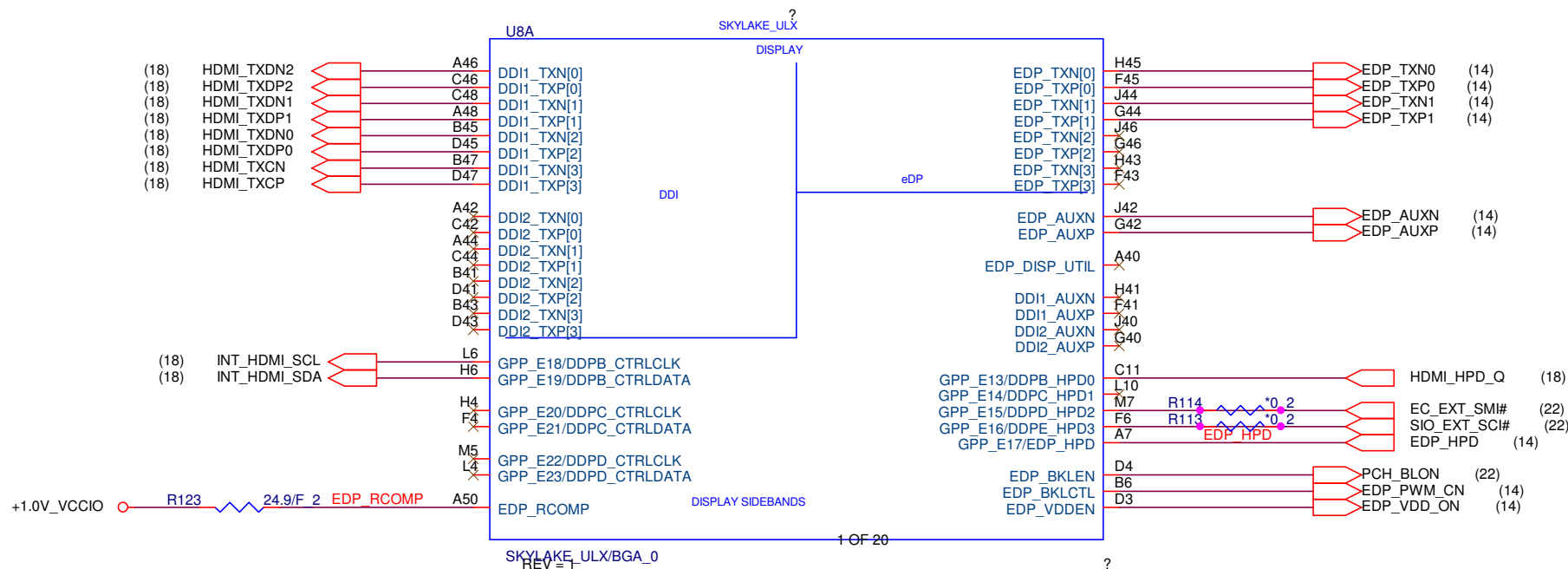


# NB12.5 Block Diagram





WWW.AITECH1.RU

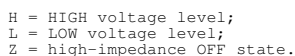


Quanta Computer Inc.

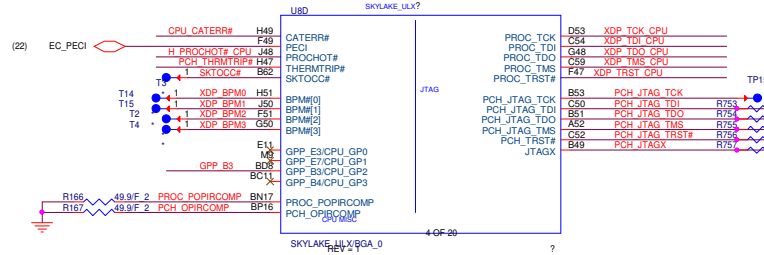
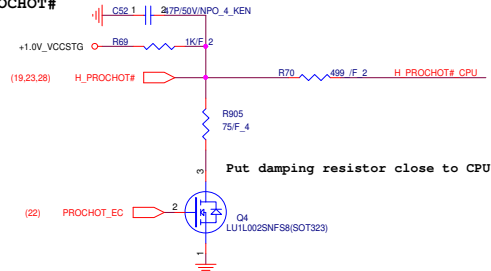
PROJECT : NN6

Size	Document Number	Rev
	KBL-Y CPU (DDI/EDP)	1A

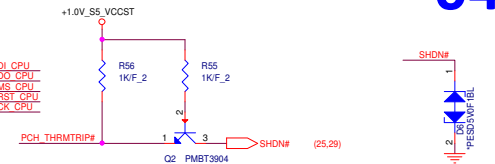
Date: Friday, August 11, 2017 Sheet 2 of 35



# PROCHOT#

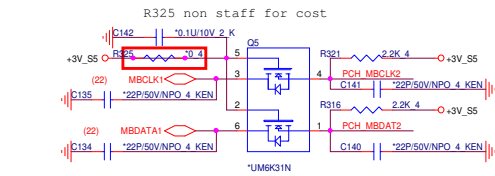


# THRMTRIP

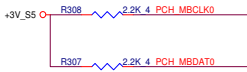


04

# SMB TO EC

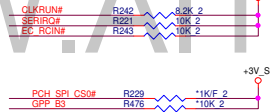
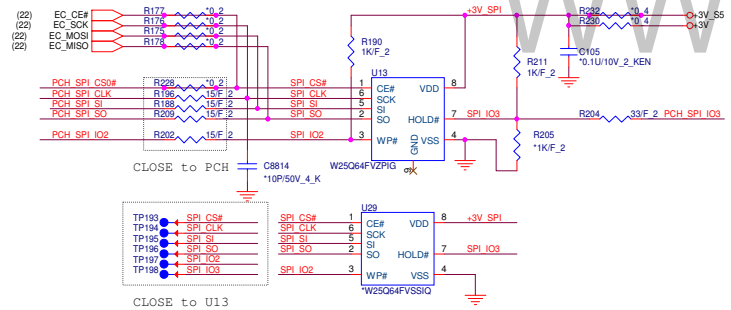


# SMB



Trace Length  
EC Side 6.5 inch  
PCH Side 8 inch

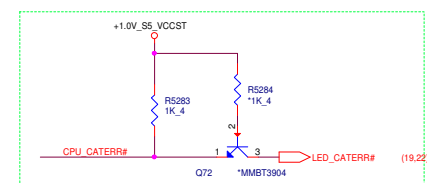
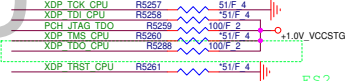
# SPI ROM for EC & BIOS



# Hardware Strap



# PCH JTAG Debug (DCI2.0)



GPP_B22 (Boot BIOS)	
PU	LPC
PD	SPI (Default IPD)

(11) NO\_REBOOT

NO\_REBOOT

+3V\_S5

TP182

TP183

TP206

TP207

Touch Pad

I2C0 TP DAT

I2C0 TP CLK

TP57

TP56

CLOSE to PCH

(17) HDA\_SYNC

(17) HDA\_BITCLK

(17) HDA\_SDOUT

(17.22) HDA\_RST#

C8788

10P/50V\_4\_K

(11) ACZ\_SPK

ACZ\_SPK

Strapping\_GPP\_B14

## Security Flash Descriptors

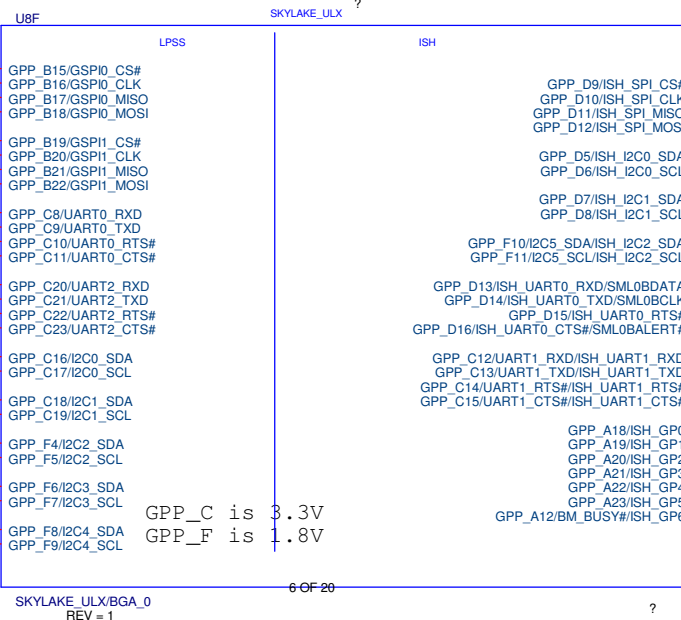
+3V\_S5

R429

\*1K/F 2

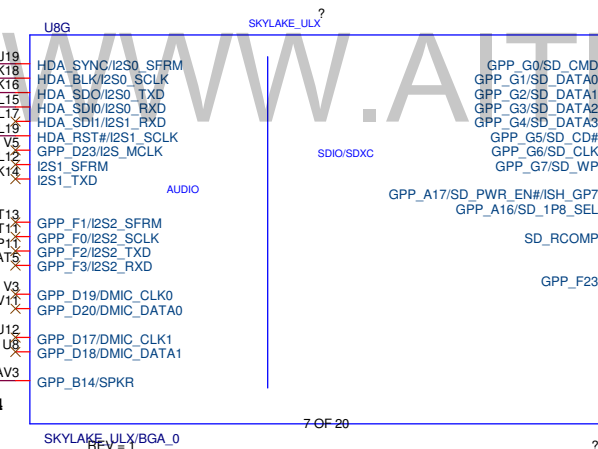
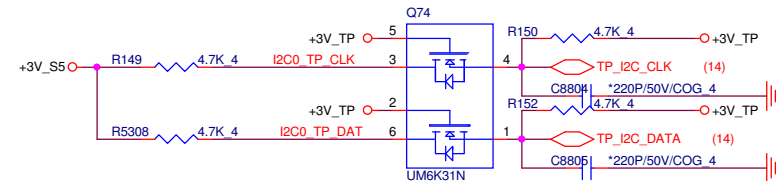
HDA\_SDOUT\_R

HDA\_SDOUT\_R (22)



INT\_TP# (14)

## I2C/Pull-up(CLG)



BOARD\_ID0

BOARD\_ID1

BOARD\_ID2

BOARD\_ID3

BOARD\_ID4

SD\_RCOMP 200/F 2

SD\_RCOMP

GPP\_F23

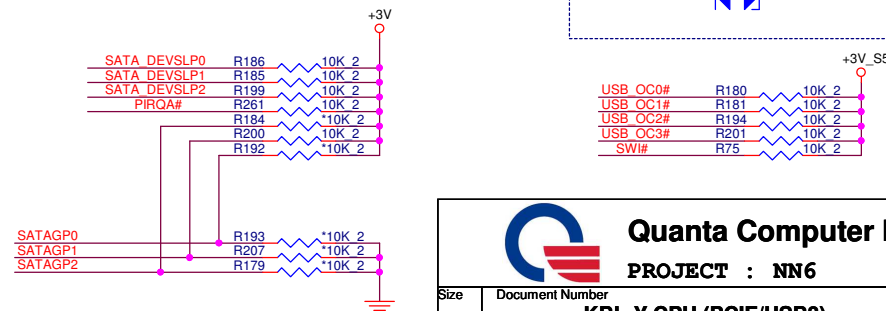
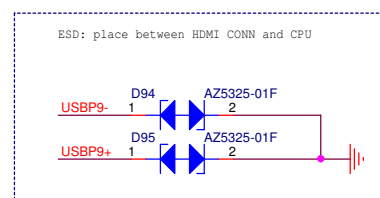
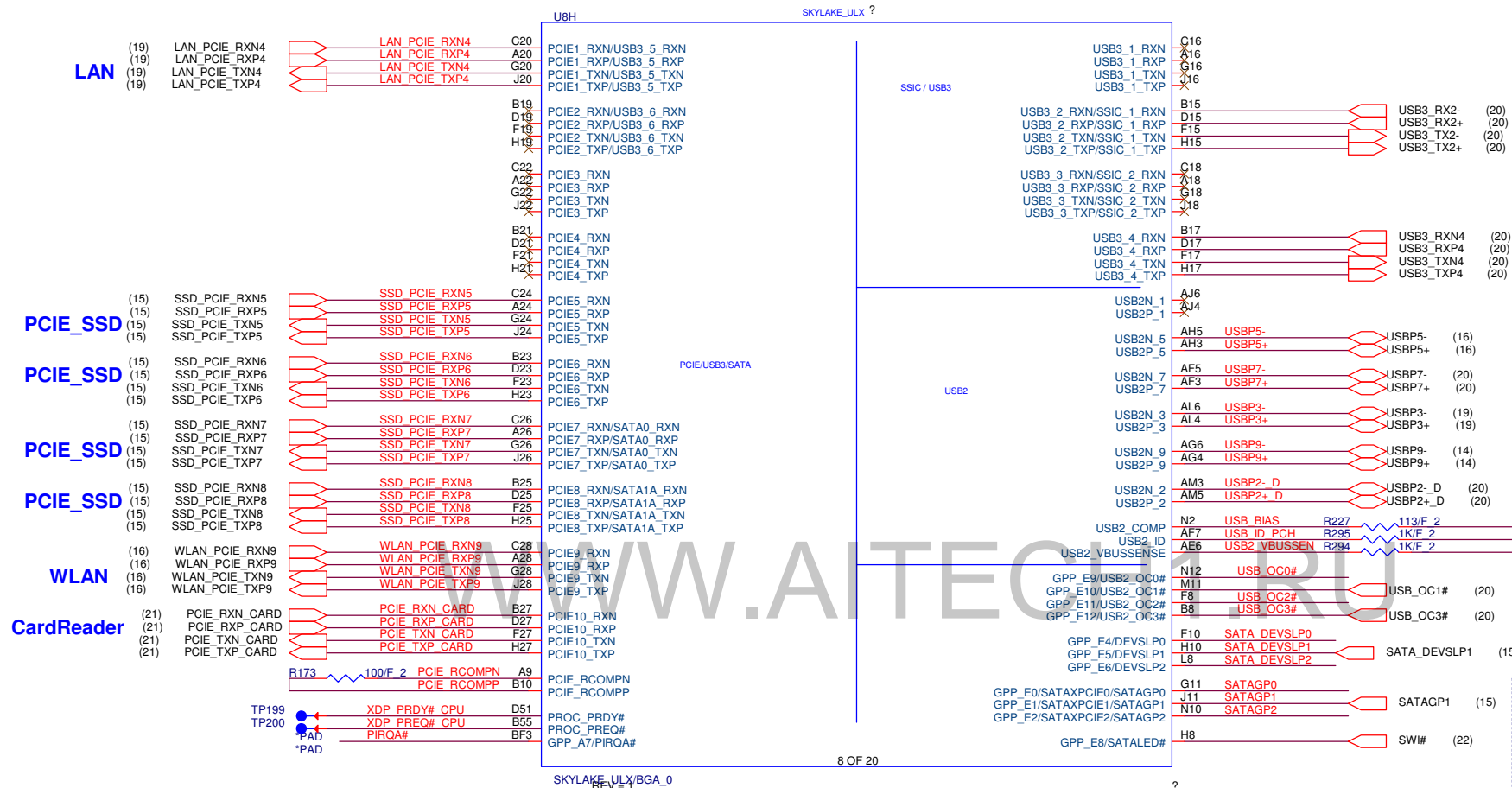
Model	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Samsung 4G K4E8E324EB-EGCF			0	0	0
Samsung 8G K4E6E304EB-EGCF			0	0	1
Hynix 4G H9CCNN8GTALAR-NUD			0	1	0
Hynix 8G H9CCNN8BJTALAR-NUD			0	1	1
Ci5 CPU	0	0			
Ci7 CPU	0	1			
m3 CPU	1	0			
Celeron CPU	1	1			

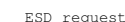
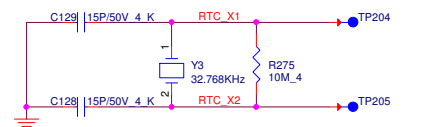


Quanta Computer Inc.

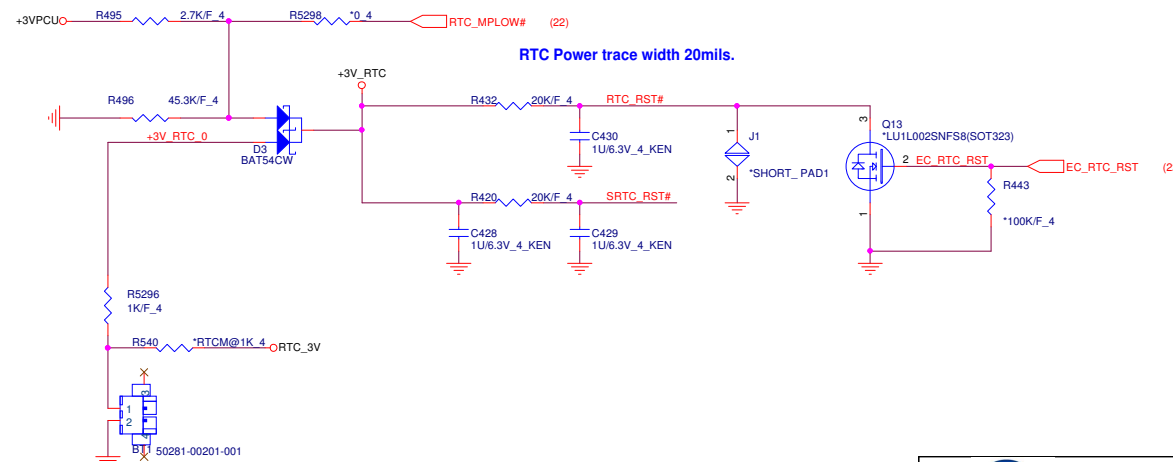
PROJECT : NN6

Size	Document Number	Rev
	KBL-Y CPU (LPSS/HDA)	1A
Date:	Thursday, September 28, 2017	Sheet 5 of 35





RTC Power trace width 20mils.



**Quanta Computer Inc.**

PROJECT : NN6

Number **KBL-Y CPU (CSI2/RTC/CLK)**

Size

Document Number

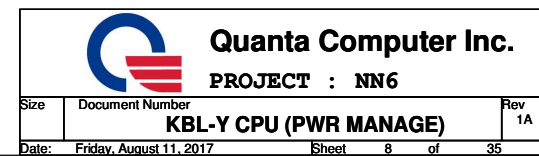
**KBL-Y CPU (CSI2/RTC/CLK)**

Date: Friday, August 11, 2017

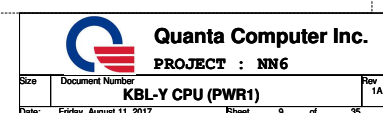
Sheet

of 3







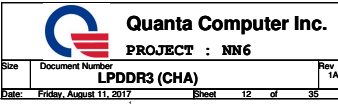


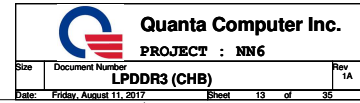
For Load switch <=65usec full load ready

## Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION NO STALL		CFG0 R54 *1K/F 2
CFG4 eDP Enable	DISABLED	ENABLED	CFG4 R53 *1K/F 2
SPKR / GPP_B14	ENABLED	DISABLED	(5) AC2_SPK R257 *1K/F 2 → 3V
GPIO_MOSI /GPP_B16	ENABLED	DISABLED	(5) NO_REBOOT R234 *1K/F 2 → 3V
SMBALERT# /GPP_C2	ENABLED	DISABLED	Already Pull-high on Page.4
Boot BIOS Strap Bit /GPP_B22	LPC	SPI	(default:SPI) Page5 Reserve PU1K
SML0ALERT# / GPP_C5	ESPI	LPC	Already Pull-high on Page.4(default:LPC)
SML1ALERT# / PCH0T# / GPP_B23			Already Pull-high on Page.4
SPI0_MOSI (PCH_SPI_S0)			Already Pull-high on Page.4
SPI0_MISO (PCH_SPI_S0)			Already Pull-high on Page.4
SPI0_IO2 (PCH_SPI_IO2)			Already Pull-high on Page.4
SPI0_IO3 (PCH_SPI_IO3)			Already Pull-high on Page.4
HDA_SDO/ I2S_TXD0	DISABLED	ENABLED	Already Pull-high on Page.5
Security Flash Descriptors			
DDPB_CTRLDATA / GPP_E19	ENABLED		Used on HDMI DDC
DDPC_CTRLDATA / GPP_E21			No Used







# Camera For EMI close to connector

CLOSE to CN6

$$\text{Fuse Rating} = \text{IR}(\text{max}) / (0.75 * 0.88) = 0.251 / 0.66 = 0.383 \text{ A}$$

14

## eDP

## Camera

## eDP

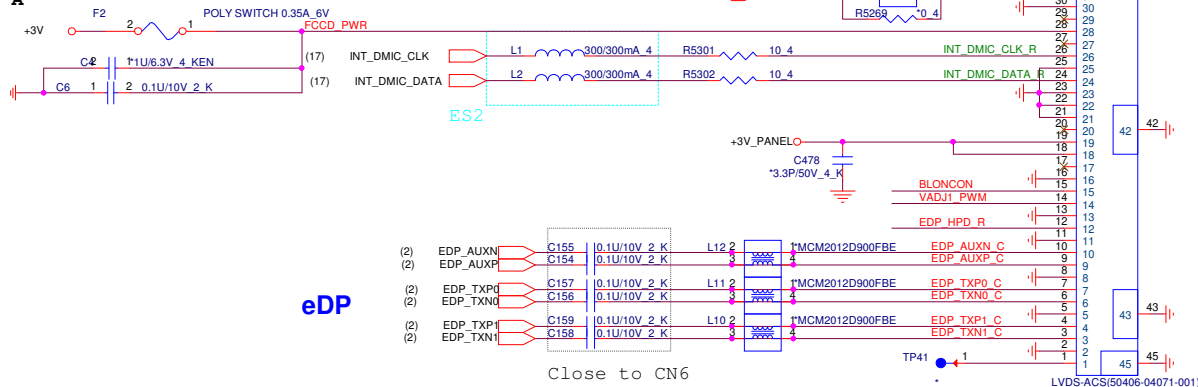
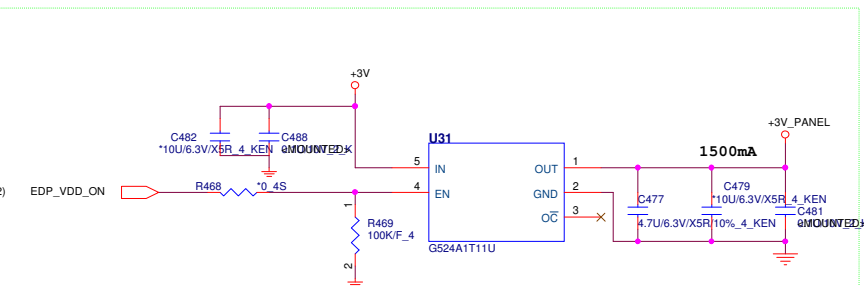
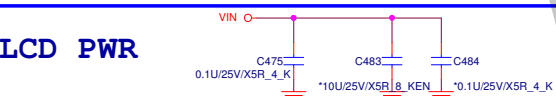
## LCD PWR

## TOUCH PAD

## T/P Board to T/P (ALPS/FFG)

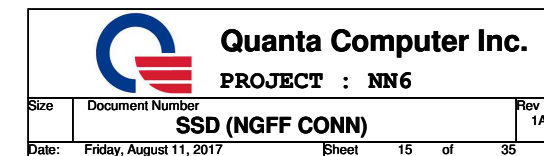
$$\text{Fuse Rating} = \text{IR}(\text{max}) / (0.75 * 0.6) = 0.01 / 0.45 = 0.022 \text{ A}$$

## I2C I/F



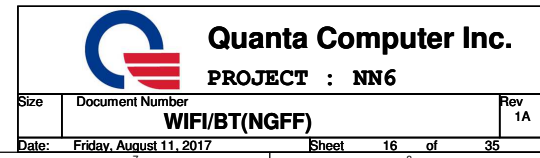


## 15

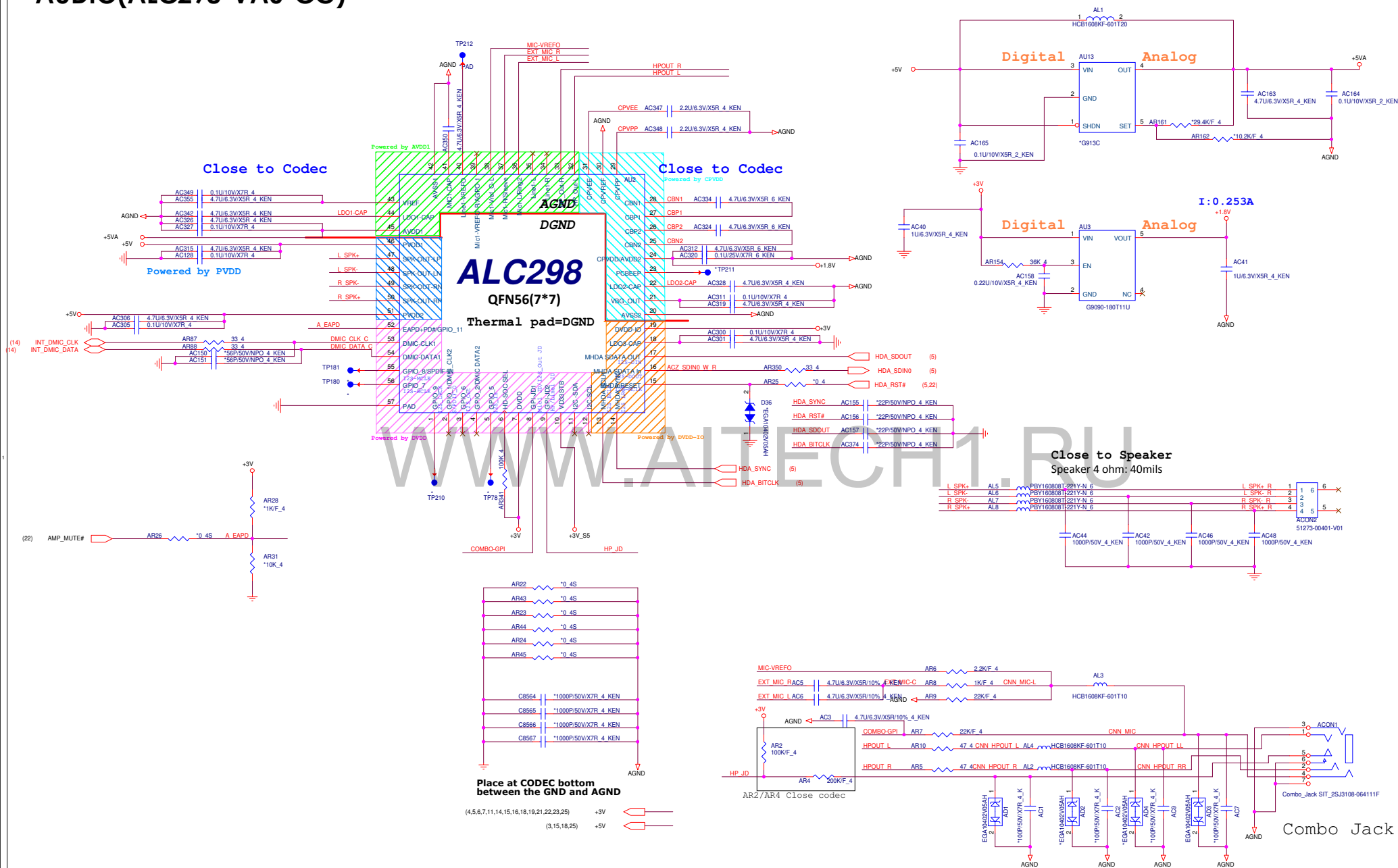




16



**AUDIO(ALC298-VA0-CG)**



## 18

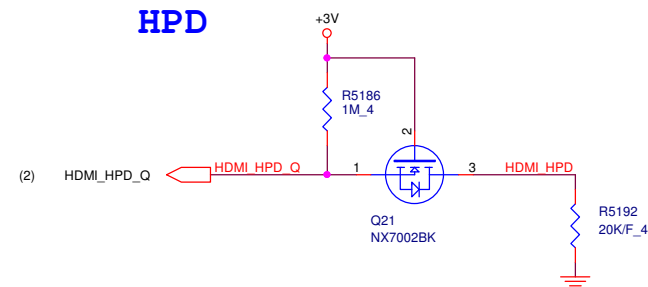
TX0 and TX2 lanes are swapped intentionally

EMI

## EMI Solution

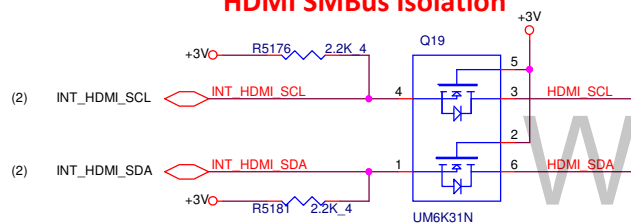
C TX2 HDMI+	R525	140/F 4	C TX2 HDMI-
C TX1 HDMI+	R524	140/F 4	C TX1 HDMI-
C TX0 HDMI+	R522	140/F 4	C TX0 HDMI-
C TXC HDMI+	R523	140/F 4	C TXC HDMI-

## HPD



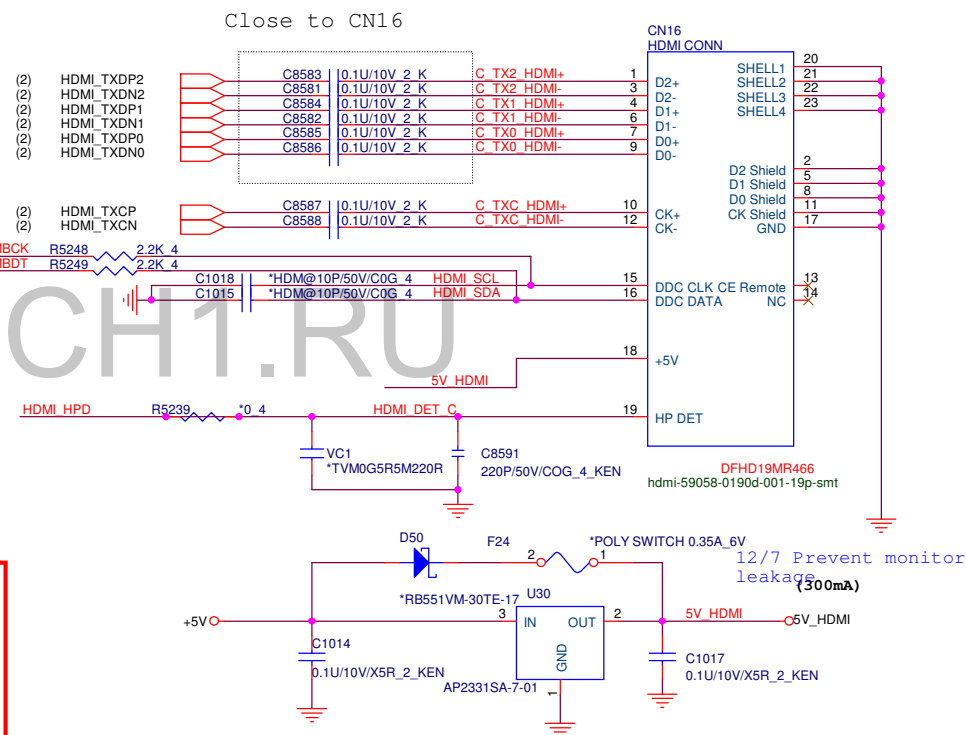
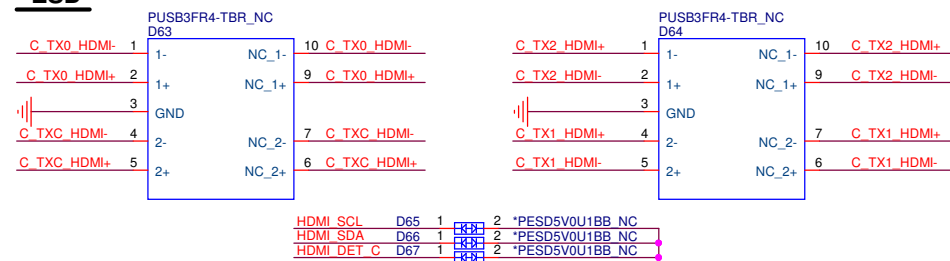
## DDC Level Shift

## HDMI SMBus Isolation



**Close to HDMI connector**

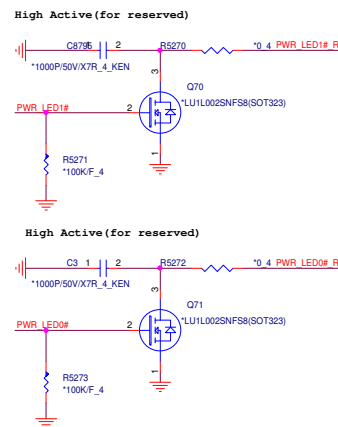
## ESD

**Quanta Computer Inc.**

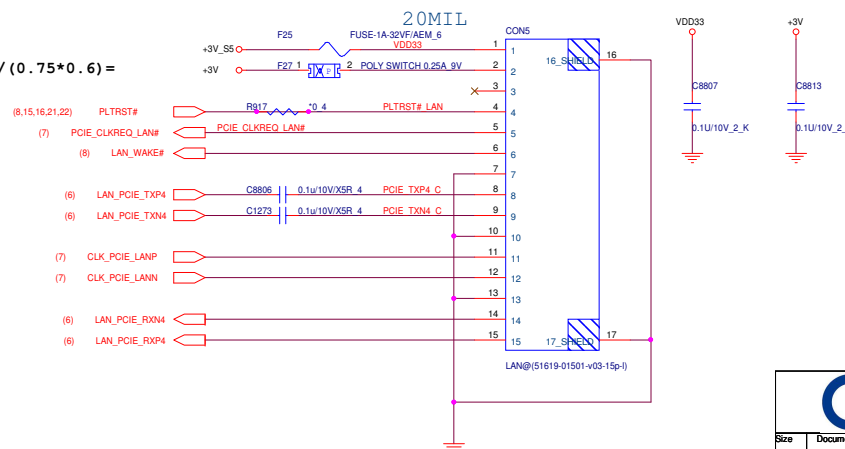
**PROJECT : NN6**

Size	Document Number <b>HDMI</b>	Rev 1A
Date:	Friday, August 11, 2017	Sheet 18 of 35

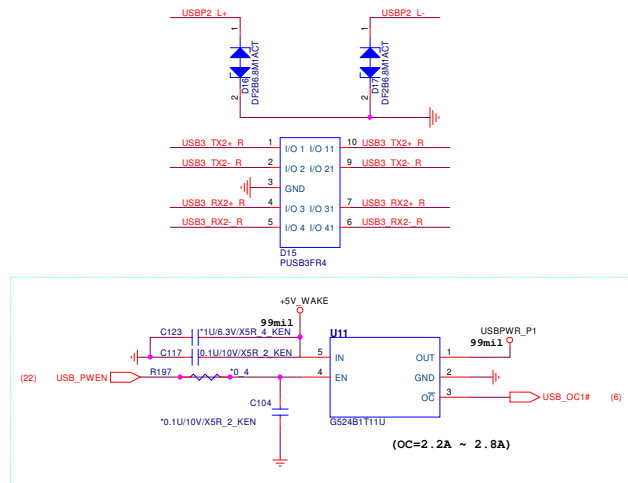
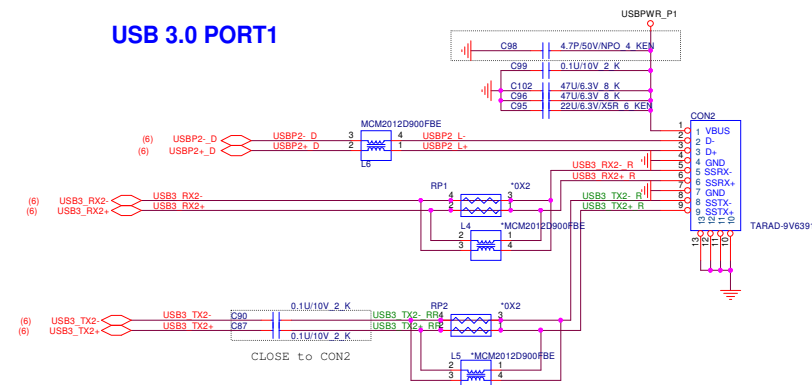
## 19



NBSWON# R	D86	*EGA10402V05AH
CAPSLED0# R	D87	*EGA10402V05AH
BATLED0# R	D88	*EGA10402V05AH
PWR LED1# R	D89	*EGA10402V05AH
PWR LED0# R	D90	*EGA10402V05AH



### USB 3.0 PORT1

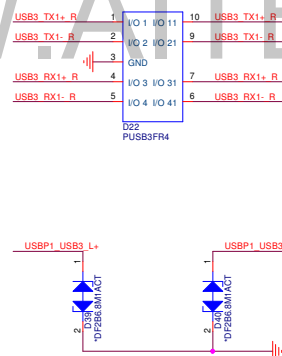
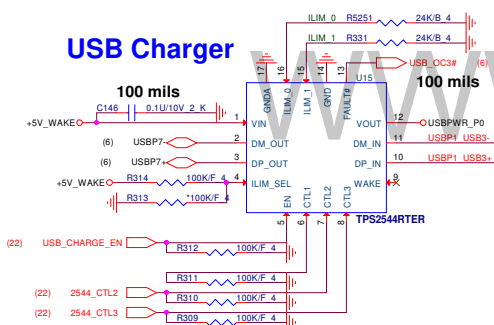


SEL	/OE	Mode
HIGH	LOW	USB Mode
LOW	LOW	UART Mode

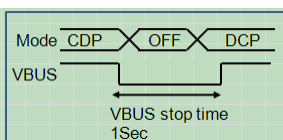
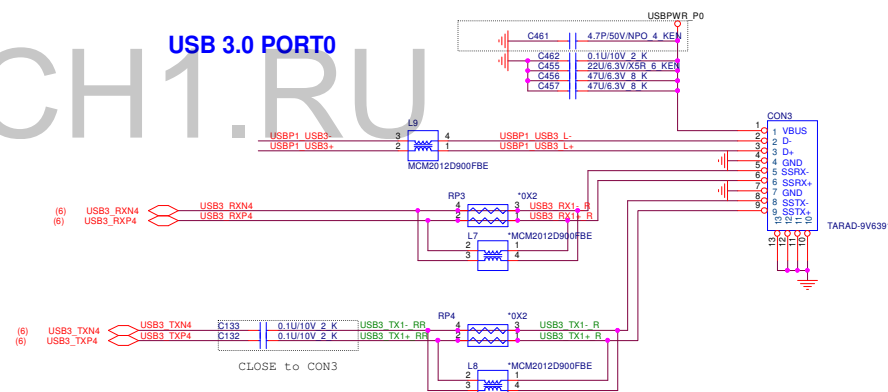
	TPS2541		TPS2544	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	

```
SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by EC
```

## USB Charger



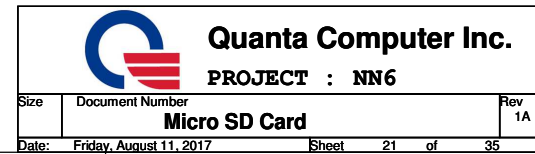
### USB 3.0 PORT0



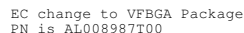
ILIM_SEL (I LIMIT(A)= 50250/R)		
HI	I_LIM_1	50250/24K=2.093A
LO	I_LIM_0	50250/24K=2.093A

USB_CHARGE_EN	CTL_1	CTL_2	CTL_3	TPS 2544 Truth Table
1	0	X	1	DCP, Auto-detect(S3/S4/S5, 1.5A)
1	1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	0	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	1	1	1	CDP (S0, 1.5A)
0	0	0	0	OUT discharge, power switch OFF

System State	USB Battery Charging Setting		
	Disable(AC and DC mode)(EN1 2 3)	Enable(AC mode)(EN1 2 3)	Enable(DC mode)(EN1 2 3)
S0	SDP (1 0 1 0)	SDP (1 0 1 0)	SDP (1 0 1 0)
S3	SDP (1 0 1 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)
S4	Charger OFF (0 0 0 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)
S5	Charger OFF (0 0 0 0)	DCP Auto (1 0 X 1)	Charger OFF (0 0 0 0)



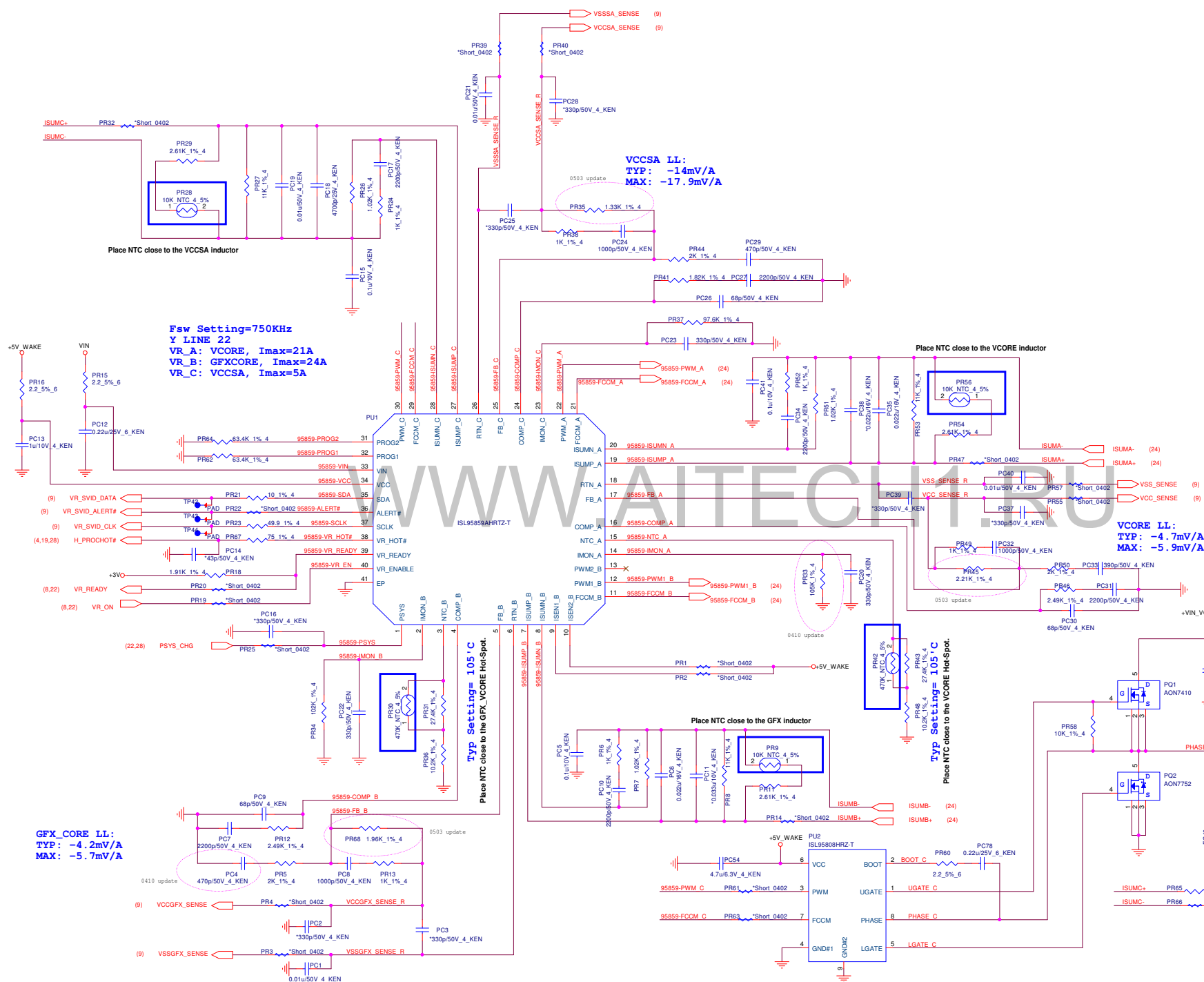
+3VPCU\_EC and +3V\_RTC  
minimum trace width 12mils.

[illegible]

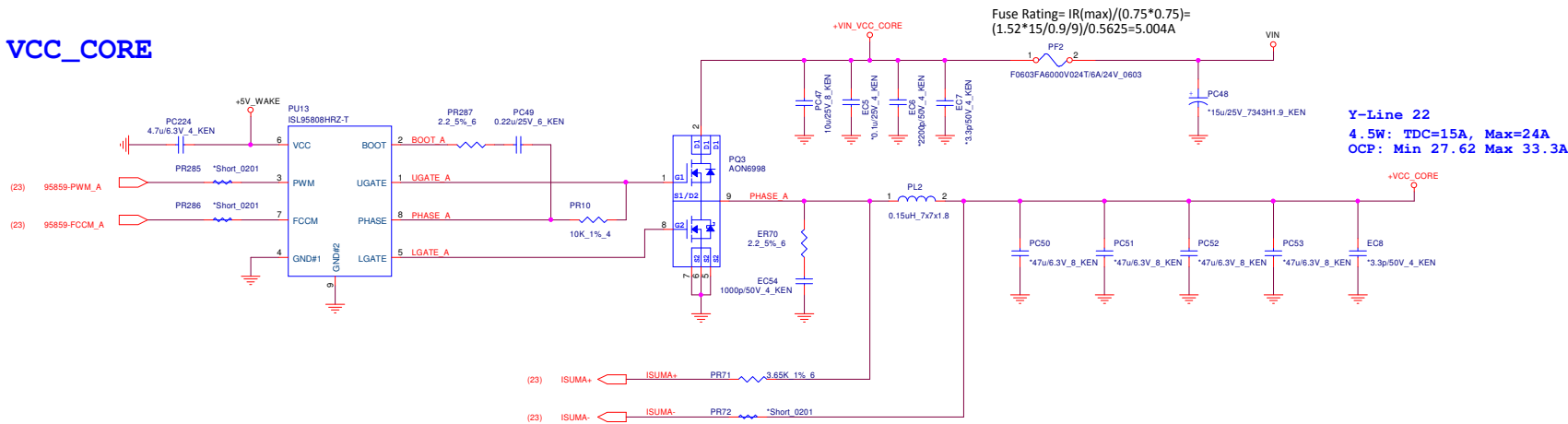
**EC PU/PD**

[illegible][illegible][illegible]

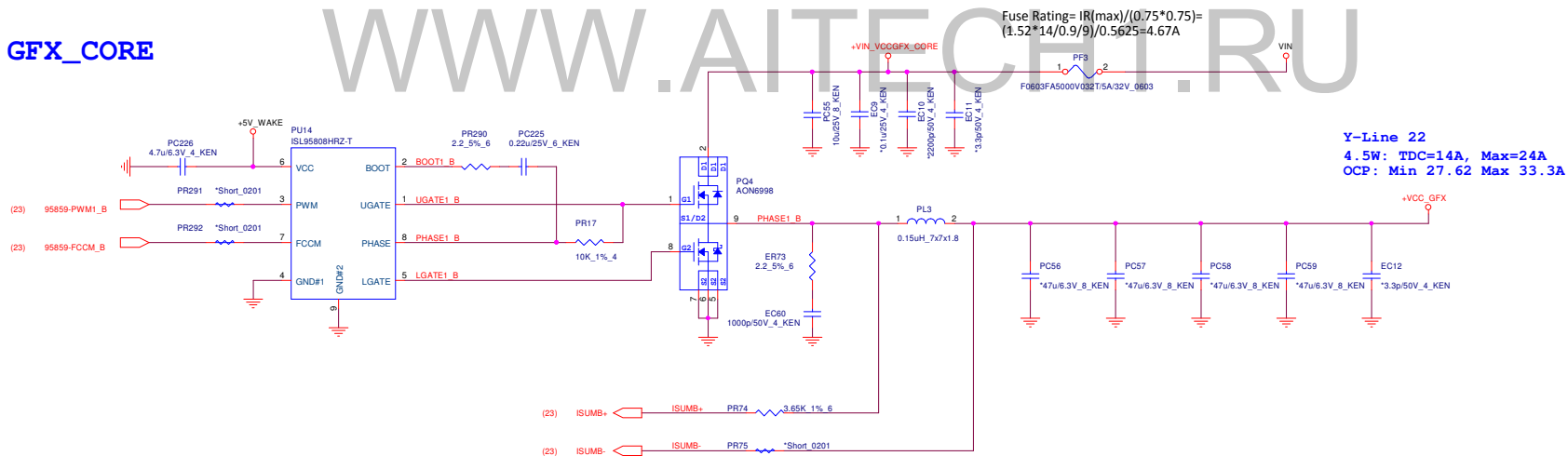




## VCC\_CORE

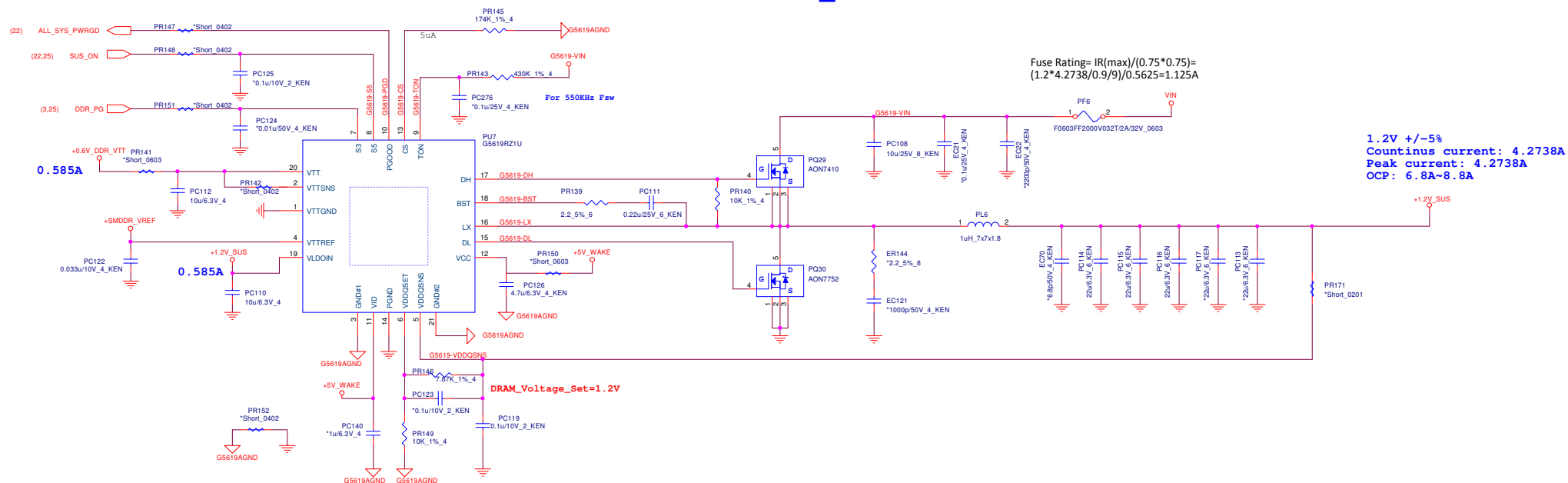


## GFX\_CORE





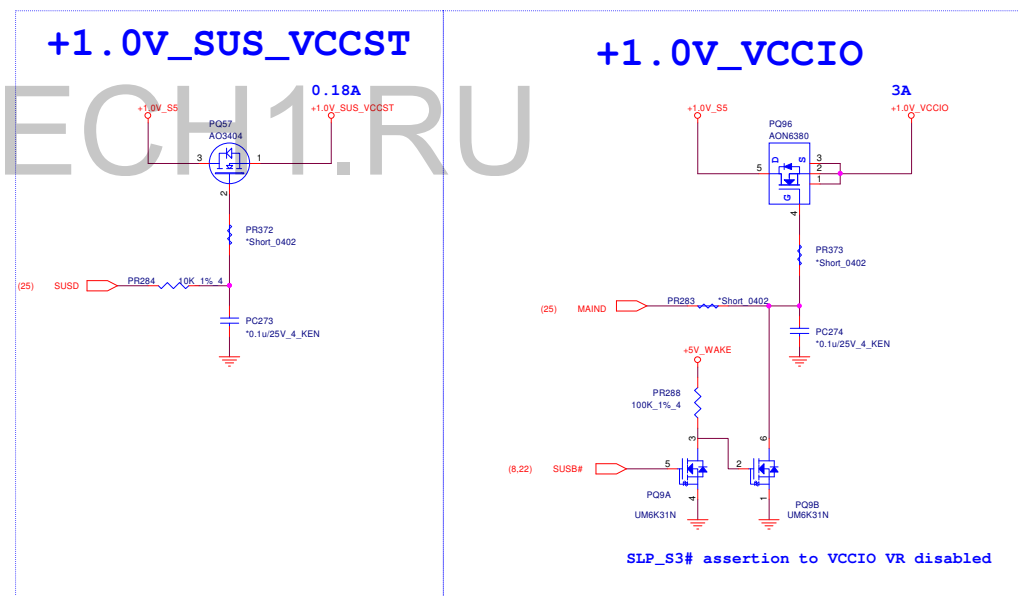
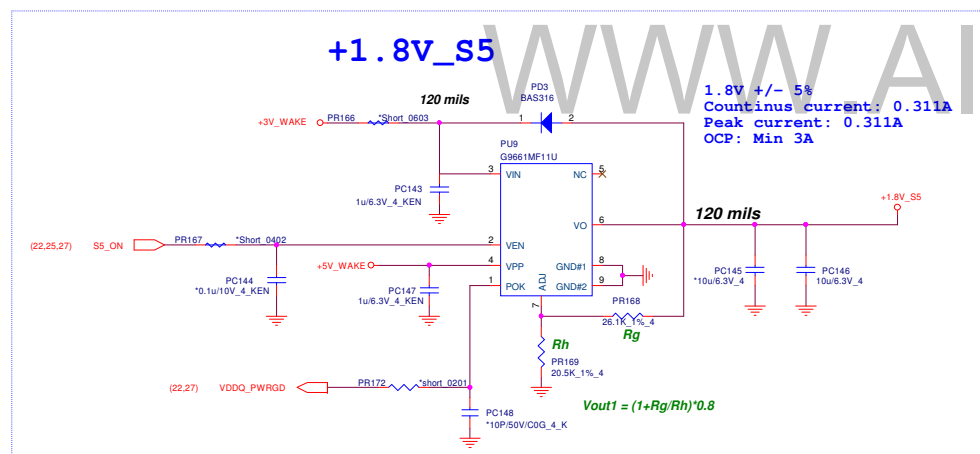
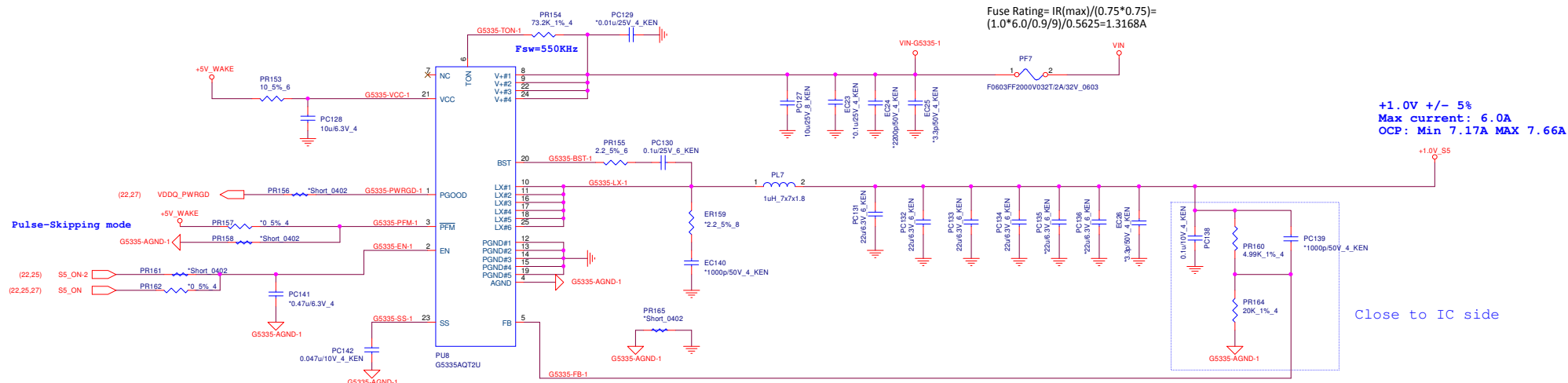
## 1.2VSUS &amp; VTT\_MEM

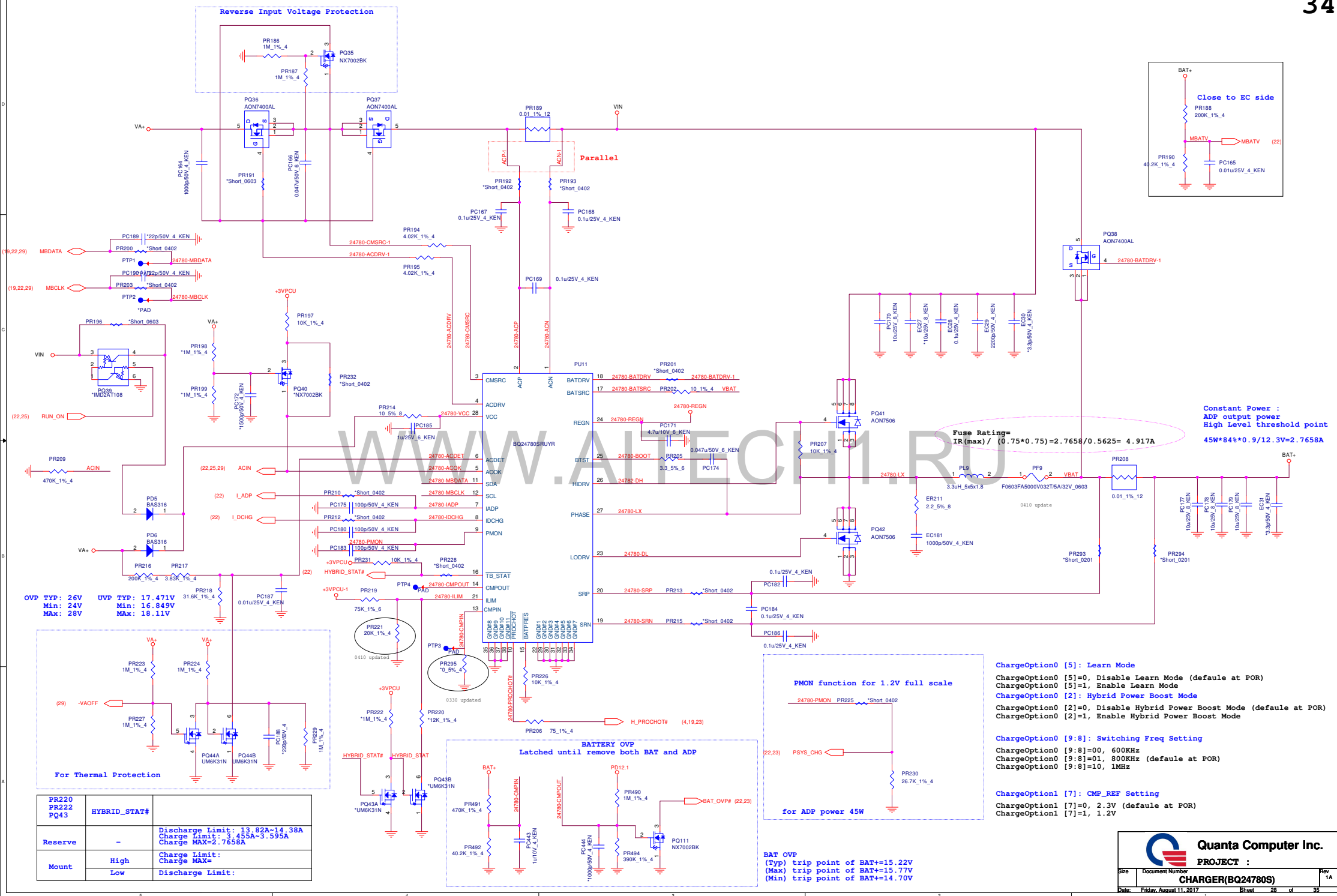


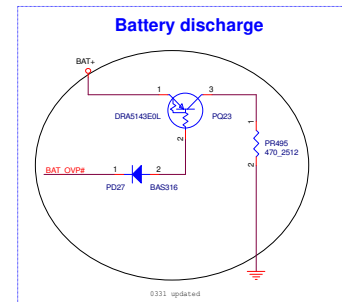
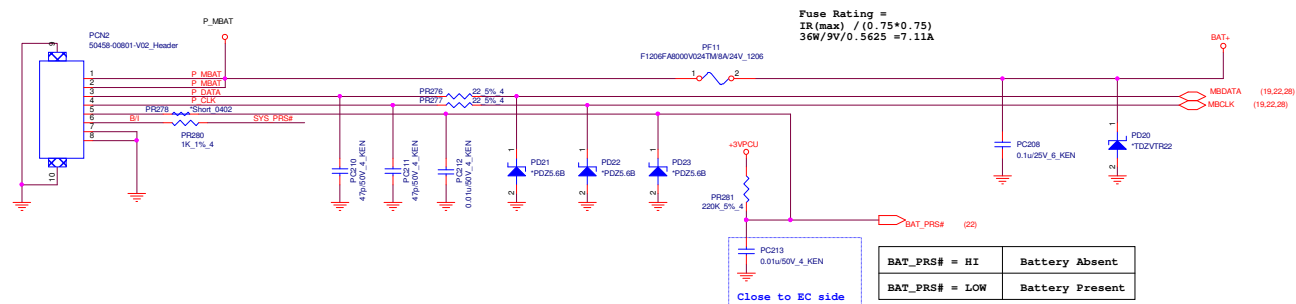
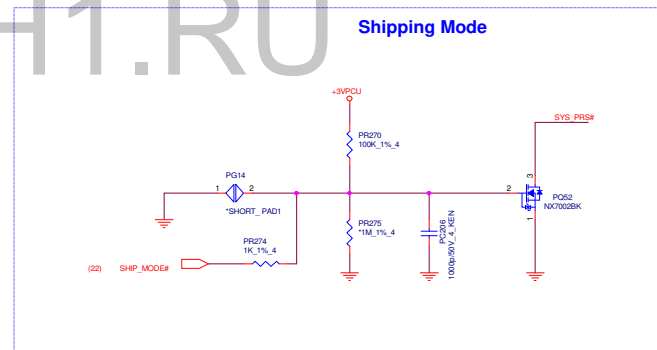
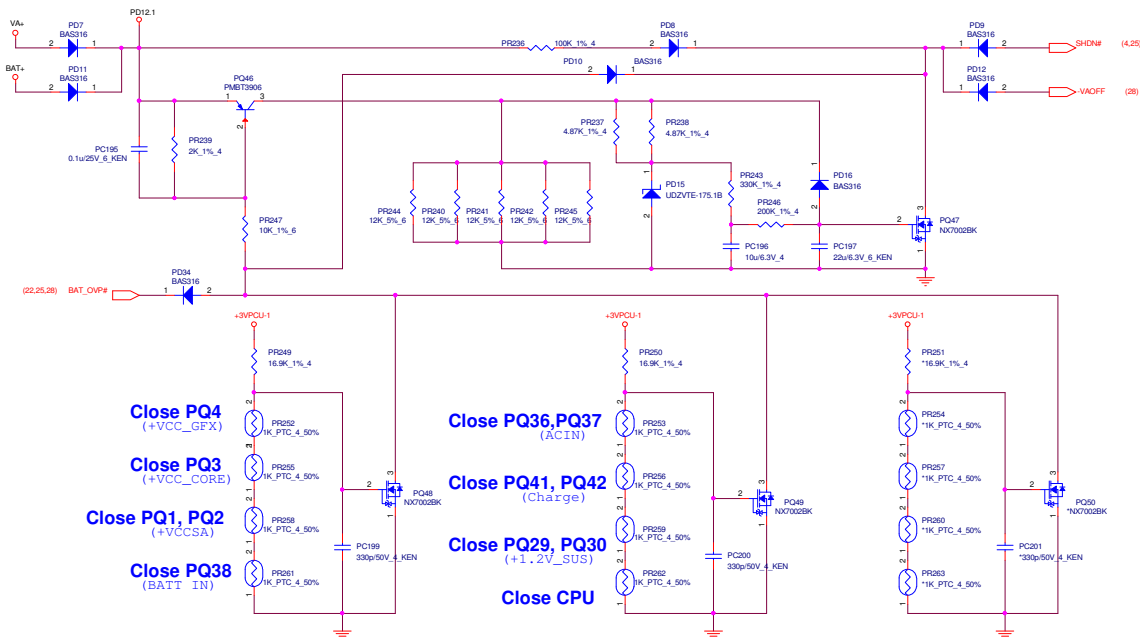
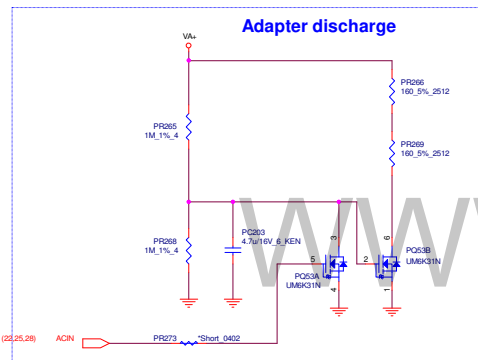
STATE	S3	S5	1.35VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

WWW.AITECH1.RU

+1.0V\_S5



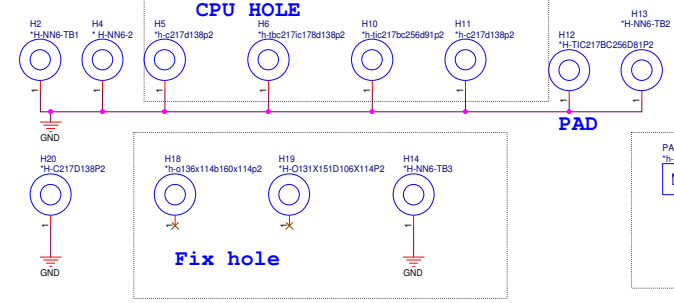


[illegible]

BAT_PRS# = HI	Battery Absent
BAT_PRS# = LOW	Battery Present



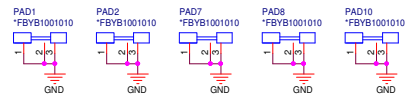
SCREW HOLE



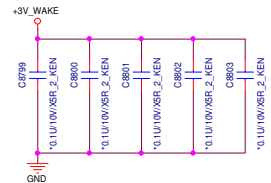
For ESD's requirment

30

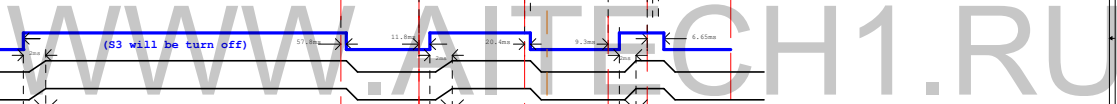
CLIP SHIELDING (CPU)

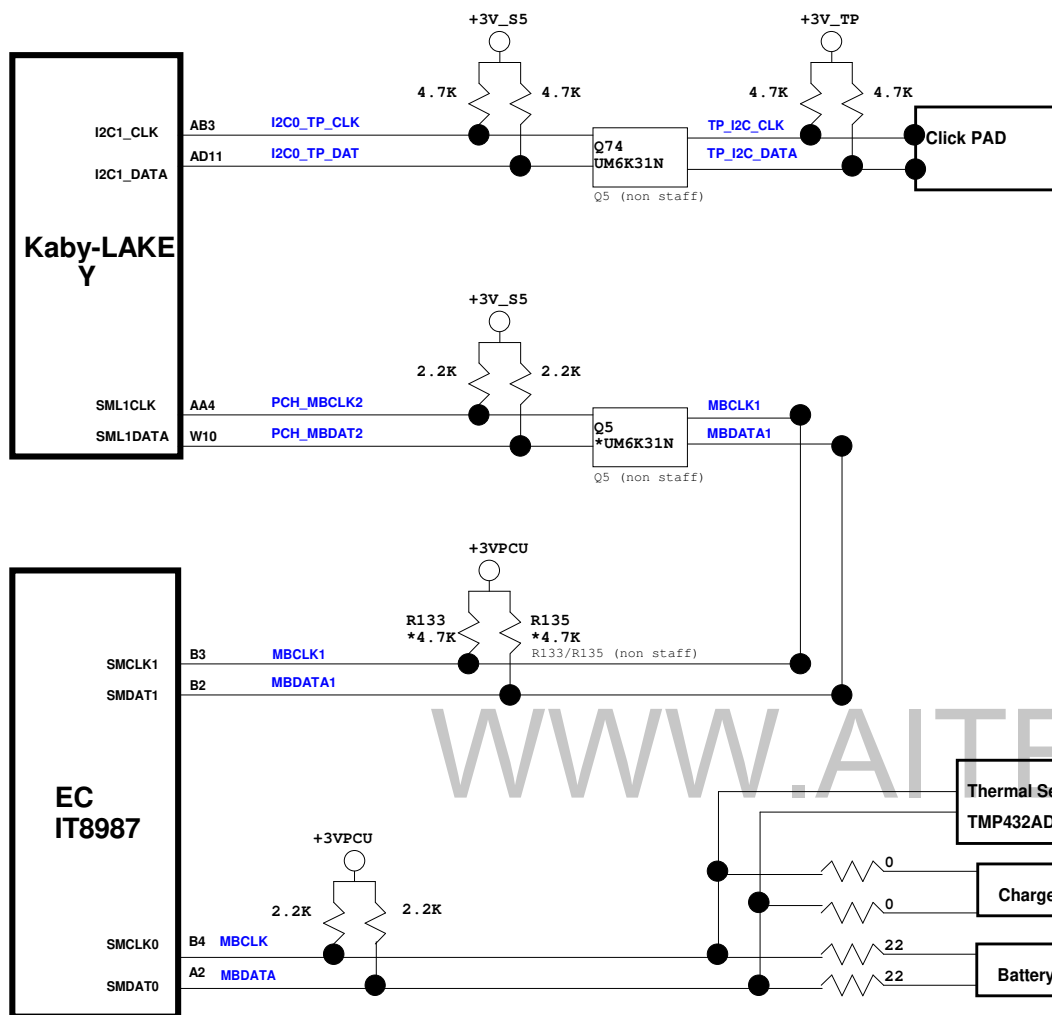


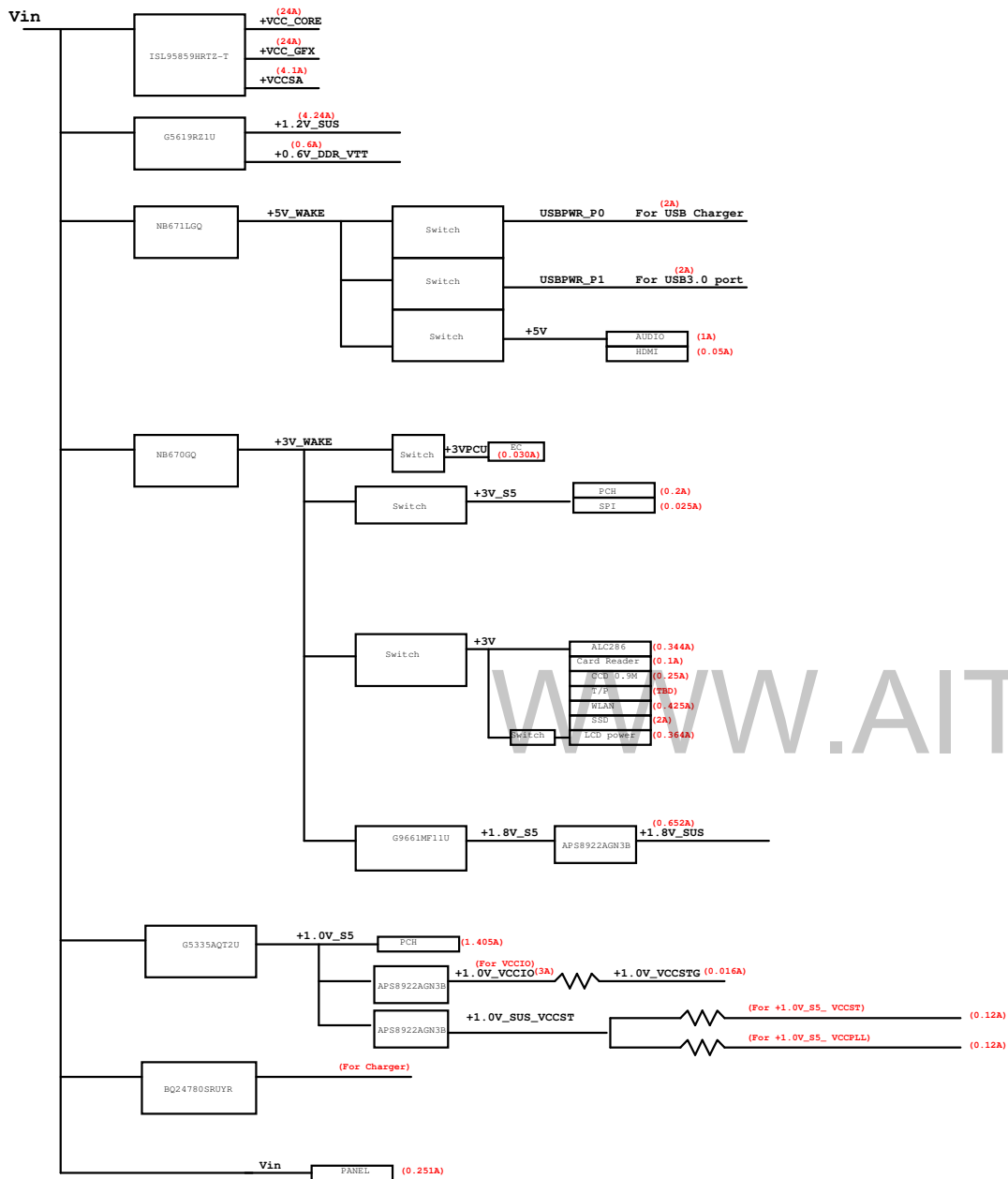
35



WWW.AITECH1.RU







OS status	S0	S3	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	S5 S4 (Win10 off) Charge Enable	S5 S4 (Win10 off) Charge Disable
RUN_ON	H	L	L	L
+3V	H	L	L	L
+5V	H	L	L	L
+0.6V_DDR_VTT	H	L	L	L
+1.8V_A	H	L	L	L
+VCCSA	H	L	L	L
+VCC_GFX	H	L	L	L
+VCC_CORE	H	L	L	L
+1.0V_VCCIO (+1.0V_VCCSTG)	H	L	L	L
SUS_ON	H	H	L	L
+1.2V_SUS	H	H	L	L
+1.8V_SUS	H	H	L	L
+1.0V_SUS_VCCST	H	H	L	L
S5_ON	H	H	L	L
+1.8V_S5	H	H	L	L
+3V_S5	H	H	L	L
+1.0V_S5	H	H	L	L
EC_WAKE_ON	H	H	H	L
+3V_WAKE	H	H	H	L
+5V_WAKE	H	H	H	L
+3VPCU-1	H	H	H	H
+3VPCU	H	H	H	H



**Quanta Computer Inc.**

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**POWER MAP**

Change history (PP to MRT)

	 <b>Quanta Computer Inc.</b> PROPERTY : 8866	
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